Chemistry 628
University of Wisconsin

**Lab Unit 5: The Lock-in Amplifier**

In this lab unit you are going to construct a lock-in amplifier and use it to measure the small signal from a photodiode exposed to light from an LED. The lock-in amplifier is a good application of a useful circuit that requires both analog and digital devices. You will need to understand and use: analog filters, amplifiers, comparators, voltage controlled oscillators, phase detectors, phase locked loops, multipliers, flip flops, and up-down counters, in order to get your lock-in to work. The entire circuit uses 16 different integrated circuits (ICs) so its construction on a breadboard would be a wiring nightmare. To save you this trouble, you will be given a printed circuit board with all of the ICs loaded. You will complete the board by selecting and adding the appropriate resistors and capacitors so each module of the lock-in functions properly.

**Background** The lock-in amplifier is a useful electronics instrument for aiding the measurement of DC or slowly varying signals that are overwhelmed by large amounts of noise. The signals can be generated by a variety of detectors including photodiodes and photomultiplier tubes for the measurement of light, thermistors and thermocouples for the measurement of temperature, and direct measurement of current or voltage in electrochemical applications. Regardless of the type of measurement, the lock-in amplifier works by limiting the detection bandwidth in a way that preserves the desired signal while reducing the total amount of noise. A well designed detection system including a lock-in amplifier can extract a clean signal from noise that is up to 100,000 times greater in amplitude.

Figure 1. shows a typical experimental set up using a lock in amplifier. The signal must be modulated at a frequency suitable for the measurement. The modulation frequency is usually above 100 Hz to minimize 1/f noise. The modulation frequency must also be selected away from any environmental noise frequencies, and must be greater than any of the slow variations in the signal that you are trying to measure. Typical modulation frequencies range from 1 to 100 kHz.

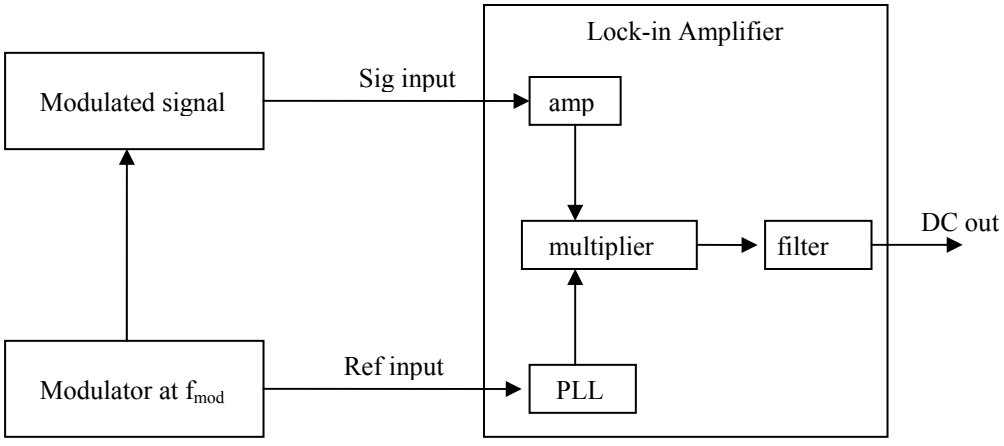



Figure 1. Block Diagram of a Lock-in Amplifier Set Up

The modulated signal is directed to the signal input of the lock-in amplifier where it is filtered by a high pass filter to remove any DC component to the signal and amplified if necessary. Included in this signal is all of the noise within the bandwidth of the detector. A reference signal at the modulation frequency is directed to the reference input of the lock-in amplifier. A good lock-in will use a phase locked loop to track this reference frequency. The phase locked loop will generate a clean reference signal at the modulation frequency, even if the reference itself is noisy, that follows any frequency variations in the modulator.

The reference signal and modulated signal are then multiplied together and sent to a low pass filter. The multiplier-filter combination is where the bandwidth narrowing takes place. Consider a single frequency component in the signal input described as $V_s=V_s\cos(\omega_s t)$ and the reference input of $V_r=V_r\cos(\omega_r t+\varphi)$ where $\varphi$ is the relative phase of the two inputs. The multiplier provides an output of $\frac{V_s \times V_r}{2}\{\cos[(\omega_s+\omega_r)+\varphi] + \cos[(\omega_s-\omega_r)+\varphi]\}$. The sum frequency component is easily removed by the low pass filter. The difference frequency component can also be removed by the low pass filter provided the difference frequency is outside the bandwidth of the low pass filter. The only signals that would not be attenuated by the filter would be signals close to the frequency and phase of the reference. The signal that you are interested in meets these criteria. Most of the noise does not.

As an example consider a low pass RC filter using a 1 uF capacitor and 1 M resistor. This gives an RC time constant of 1 sec and an effective bandwidth of 1/RC or 1 Hz. All noise outside of 1 Hz of the modulation frequency is effectively eliminated by the lock-in. The bandwidth without the lock in could be as high as 1MHz, and noise amplitude is reduced as the square root of bandwidth, so the lock-in decreases the noise by a factor of 1000. The penalty for using long time constants to decrease noise is the slower response time of the measurement. You can only detect changes in your signal that occur on time scales slower than the time constant of the filter.

**Construction of the Lock-in Circuitry** The accompanying circuit diagrams outline the design of the lock-in amplifier that you will be putting together. It is best to put the circuit together in a stepwise manner and verify the function of each section as you put it together. You will design your circuitry around 8 kHz as a good modulation frequency. Use the function generator to generate a sin wave at this frequency with a p-p voltage of about 100 mV.

*Reference Channel Input* The first stage of the reference input is a simple high pass filter. This filter is used to remove any DC component to the reference signal. The filter also sets the input impedance for the reference input. To get a high input impedance choose R1 to be 1 MΩ then choose an appropriate capacitor so that you do not attenuate the reference at the modulation frequency.

The LF356 is an FET input operational amplifier is used as a non inverting amplifier to amplify the reference signal. Use R3 and R2 to set the amplification to 10 but recognize that this may be adjusted later. Use the potentiometer attached to the LF356 to remove any DC offset. The LM311 comparator is used to generate a 0-5 V square wave at the reference frequency. The 10 K pull-up resistor is already on the board. Use a 10K resistor for R4. Choose R5 to add hysteresis to the comparator to prevent extra oscillations.

Sketch the reference signal at test points 1 through 4 in your notebook. Does each waveform make sense?

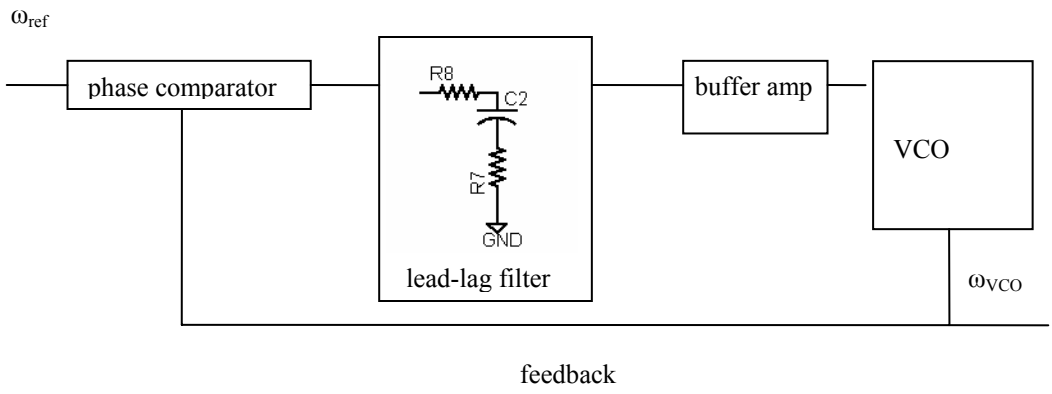
*Divide by 2 Phase Locked Loop* The 74C74 is a D-type flip flop used to divide the reference frequency by 2. Confirm its working properly by looking at TP5.

The LM13700 transconductance operational amplifiers are used to make a voltage controlled oscillator. Construct the VCO according to the circuit diagrams attached. Test the VCO by applying a voltage source to pin 3 of the OP27 follower circuit (note: the right side of C2 is connected to pin 3 of the op amp so that receptacle can be used for the applied voltage). This voltage source will be used to control the frequency of the VCO. Monitor the VCO frequency at TP9 and TP10. Measure the frequency range of the VCO with an applied voltage from 0 to 5 V. The applied voltage should be measured at TP8. Be sure your VCO oscillates at half of the reference frequency when the applied voltage is less than 5 V. If not, you will have to change components. The specification sheet of the LM13700 that describes this VCO circuit gives the oscillation frequency as $f_{osc} = \frac{I_C}{4 I_A R_{12} C_3}$.

Hook up the LM311 comparator by placing a 10 K resistor in R14. The comparator converts the square wave output of the VCO to logic levels (0-5V) maintaining the frequency. Adjust the applied voltage so that the VCO oscillates very close to half of the reference frequency. This is best done by monitoring the signals at TP5 and TP11 simultaneously and adjusting the VCO voltage.

Although the CD4046 is a complete phase lock loop in itself, in this circuit you are using only the phase comparator component of the chip. Look at the outputs of the CD4046 by monitoring TP6 and TP7 as you gently adjust the VCO frequency. Try to sketch the output at TP6 and TP7 when the VCO frequency is slightly higher than half the reference frequency and when the VCO voltage is slightly lower than half the reference frequency.

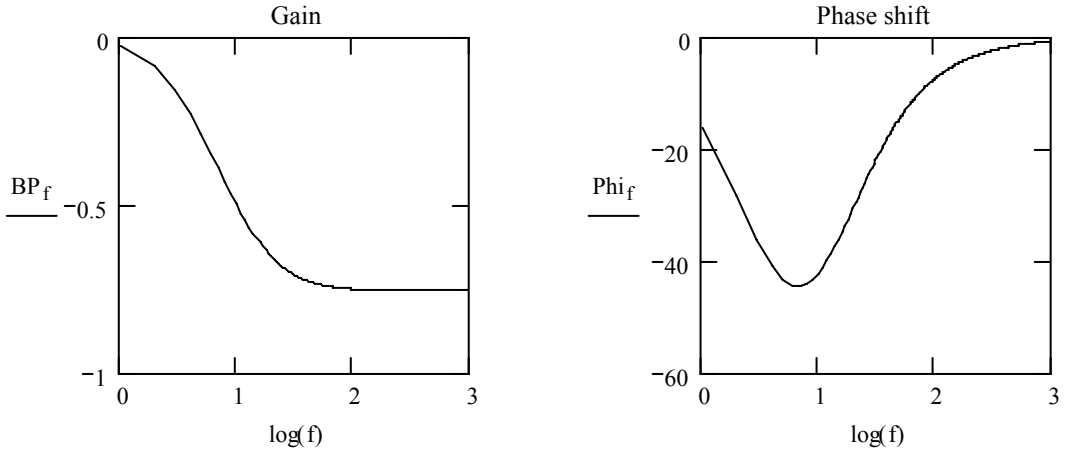
Now you need to close the loop by connecting up the low pass filter after the phase comparator. The low pass filter used is a lead-lag type filter which helps control the phase shift. In a simple low pass filter the phase can shift to $90^o$ which is problematic in this circuit since the VCO also contributes a $90^o$ phase shift. The sum of the two can give a $180^o$ phase shift which will lead to instability in the feedback system. Let's take a detailed look at the phase lock locked loop and consider the loop gain and phase shifts associated with the loop.




The phase comparator provides an output voltage proportional to the difference in frequency of the two inputs. There is no phase shift associated with the phase detector. The lead lag filter has a complex transfer function given by:

$$\frac{1+i\omega R_7 C_2}{1+i\omega\left(R_7 C_2 + R_8 C_2\right)}$$

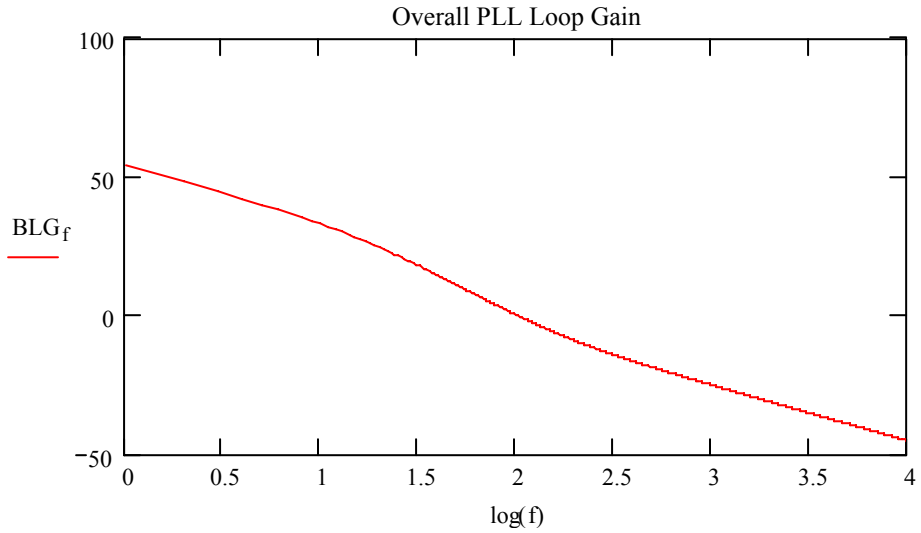
At high frequencies this simplifies to a simple voltage divider between R7 and R8. More importantly for us is that if you choose R8 that is about 4 to 5 times larger than R7 the maximum phase shift of the filter is only about 45°. This is shown in the following Bode plots for a lead lag filter using R7=1M, R8=4.7 M, and C2=0.01 uF.




Since the loop gain of the buffer amplifier is unity, the op amp will not introduce a phase shift until the frequency reaches the gain-bandwidth product, which is well above any frequencies that

we are concerned with here. In other words the feedback loop gain will be well below unity before the op amp introduces any phase shift.

The VCO acts as an integrator and has a 1/f frequency response in its gain and a 90° lagging phase shift. Combining the maximum 45° phase shift from the lead lag filter with the 90° phase shift of the VCO, the total phase shift is 135°, which gives a comfortable phase margin of 45° in the feedback loop. An example of he overall gain of the feedback loop is shown in the following Bode Plot:




At frequencies below 10 Hz, the gain falls off as 1/f due to the VCO. After 10 Hz you see an additional roll off due to combination of the lead-lag filter and the VCO. This additional roll off is reduced when the frequency reaches about 300 Hz. This point is called a "zero" and is introduced by the lead-lag filter when ωR7C2 = 1.

You will design your lead-lag filter to have the "zero" near f= 10 Hz. Choose a capacitor of about 0.01 uF, calculate a desired value for R7 from ωR7C2 = 1, and choose R8 to be 4 to 5 times larger than R7.

Remove your applied VCO voltage and add your lead lag filter components. Confirm that your PLL is locked to half of the reference frequency.

Sketch the VCO triangle wave output at TP9, the square wave output at TP10, and the VCO square at logic levels at TP11. Measure the phase jitter in the square at TP11.

*Phase Shifter* The phase shifter uses an LM311 comparator with the VCO triangle wave at one input and an adjustable voltage at the second input. Use a 10K resistor for R17. Another 74C74 is used here to convert the LM311 output to a square wave. Note that this conversion gives a square wave that is one fourth the frequency of the reference. Monitor the signal at TP12 and TP13 as you change the potentiometer. You will have to trigger the scope with the sync out from the function generator to see what is happening at TP12 and TP13. Also look at TP13 relative to TP5 and TP4 as you change the phase potentiometer. Verify the leading edge of the

square wave at TP13 is adjustable relative to the leading edge of the square at TP4. Also verify that the square at TP13 is one fourth the frequency of the square at TP4, which is the reference frequency.

*Multiply by 4 Phase Locked Loop* This second phase locked loop is constructed similarly to the first except a 74LS193 counter is used in the feedback loop so that the VCO oscillates at 4 times the input frequency. This will get you back to your reference frequency. The R and C values used in the VCO also must be set so that the VCO oscillates at the reference frequency, which is twice the frequency of the last VCO that you constructed. This is most easily accomplished by choosing C5 as half the value you chose for C3 and construct the rest of the VCO with the same resistance values as before. Again you will construct the VCO first and then close the feedback loop of the PLL with the appropriate lead-lag filter.

Put together the VCO with the appropriate components and apply an external VCO voltage to pin 3 of the OP27 follower circuit (note: the left side of the receptacle for C4 is connected to pin 3). Monitor this applied VCO voltage at TP16. Apply voltages from 0 to 5 V volts and verify that the VCO oscillates at the reference frequency within this voltage range. Change components if necessary. Verify the signals at TP19, TP20, TP17, TP15 and TP14. Remove the external voltage. Close the loop by constructing the lead –lag filter. The same components you used in the first loop should work for this loop also. Start with those values and adjust if necessary. Your PLL should now lock on the reference frequency. Verify that you have near $360^o$ phase shift control with your signal at TP20 compared to the reference input at TP3 by changing the phase control potentiometer.

*Multiplier and Filter* The multiplier section uses an AD630 modulator/demodulator as the multiplying chip. A block diagram of the chip is included in the schematics. You can think of the chip as having an input that goes through a selectable amplifier stage where the signal is either amplified by an inverting amplifier or a non inverting amplifier and the selection is determined by the output of a comparator. The reference signal is applied to the comparator. When the reference signal is greater than 0 V, the input is amplified by the non inverting amplifier. When the reference signal is less than 0 V, the input is amplified by the inverting amplifier.

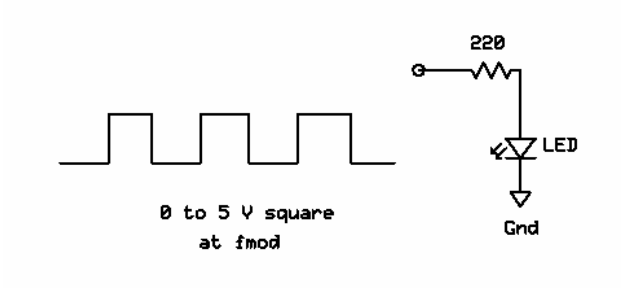
Before multiplication, the signal is passed through a high pass filter and amplified. Make the high pass filter using the same filter values in R30 and C7 as you did for the reference input at the very beginning in R1 and C1. You also need to remove the DC offset from the VCO square reference frequencies. The same RC filter values can be used here for C6 and R32. Also set the initial gain for input stage at 10 by selecting R33 = 10R31. To verify this part is working properly, apply the same input as your reference to the signal input and look at TP22 and TP23.

Measure the amplitude of the signal at TP22. Look at the output of the multiplication at TP24. Adjust the phase control. Sketch the output at TP24 when the signal and reference are exactly in phase and when the two are near $-180^o$, $-90^o$, $+90^o$ and near $+180^o$ out of phase. Predict the "average" value for the waveform in each case.

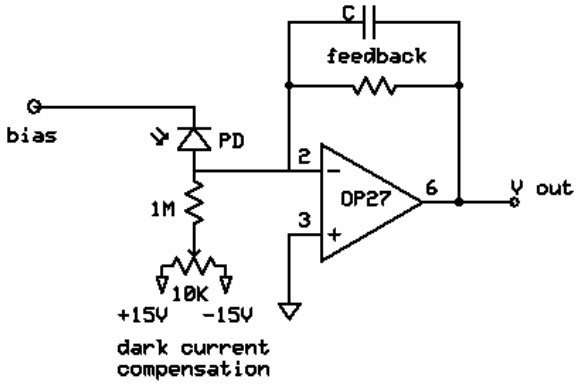
The final stage of the lock-in is the low pass filter. This stage sets the bandwidth for the noise reduction. Start by selecting R34 and C8 for a time constant of 0.1 sec. Monitor the DC output and again change the phase so that the signal and reference are near -180°, -90°, 0°, +90° and near +180° out of phase. Record the DC output in each case.

Congratulations! Your lock-in is now completed.

**Construction of the LED source/ Photodiode detection system** Set up the LED on one of the small breadboards using a simple 220 Ω resistor in series with the LED. Use your function generator to turn the LED on and off by supplying a 0-5 V square wave to the LED as shown below.




The following detection circuit is already constructed for you on the small printed circuit board. You will be setting up a modulation frequency at 8 kHz so the speed of the detection system does not have to be that high. Therefore you can set up the photodiode without biasing. A 1 MΩ and 10pF capacitor are used for the I to V feedback. These components can be changed if necessary.




Confirm that the detection circuit is working by directing the LED light onto the photodiode and looking at Vout with your oscilloscope.

**Performance Test with LED/PD** You will now look at the performance of your lock-in by using it with your LED source/photodiode detection system. Set up the LED so that it is about 1 m from the photodiode. The output of the function generator is used for the reference input of the lock-in. Since this voltage is relatively high you will have to reduce the gain of the reference channel amplifier. Remember that using the same value for R2 and R3 gives a gain of 2 for the non inverting amplifier. When you have reduced the gain, connect the reference signal to the lock-in. Also connect the output of the I to V converter to the signal input of the lock-in. You

will probably need to increase the gain of the signal channel. Connect the lock-in output to the voltmeter and maximize the signal with the phase control.

With your oscilloscope, monitor the signal at TP22 of the lock-in. You should be able to see the square wave output of the photodiode. Estimate the signal to noise ratio in this signal. Compare this to an estimate of the S/N from the output of the lock-in. Do this by making about 10 measurements and calculating the average and standard deviation in the measurement. Change the lock-in time constant to 1 sec and repeat the noise measurement.

Now make the original S/N a lot worse by replacing the red LED with the green LED. The green LED has a lower light intensity and the photodiode is less responsive to green than red. Also turn on the fluorescent desk lamp. At TP22 you can see that the signal is swamped by the noise from the desk lamp, but the output of lock-in still provides a stable DC value for the LED source.

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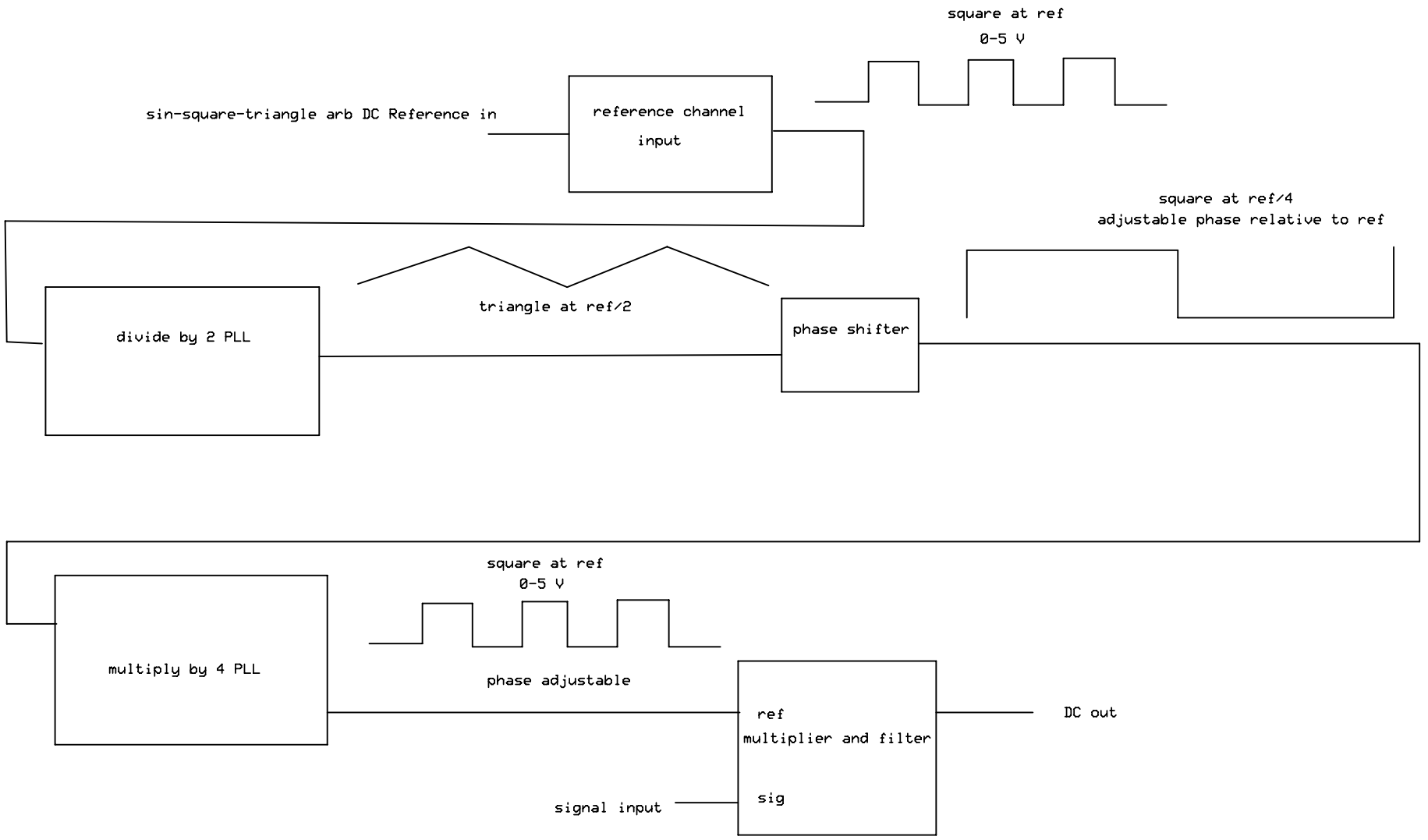

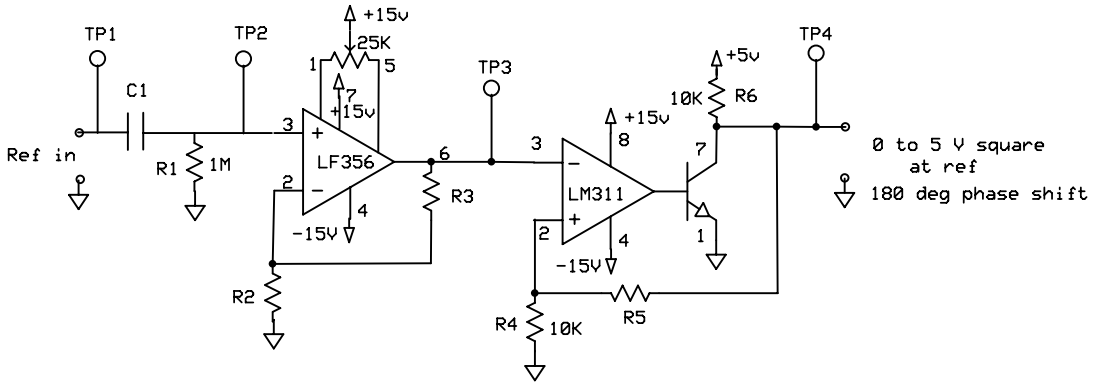


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| Reference Channel Input | | |
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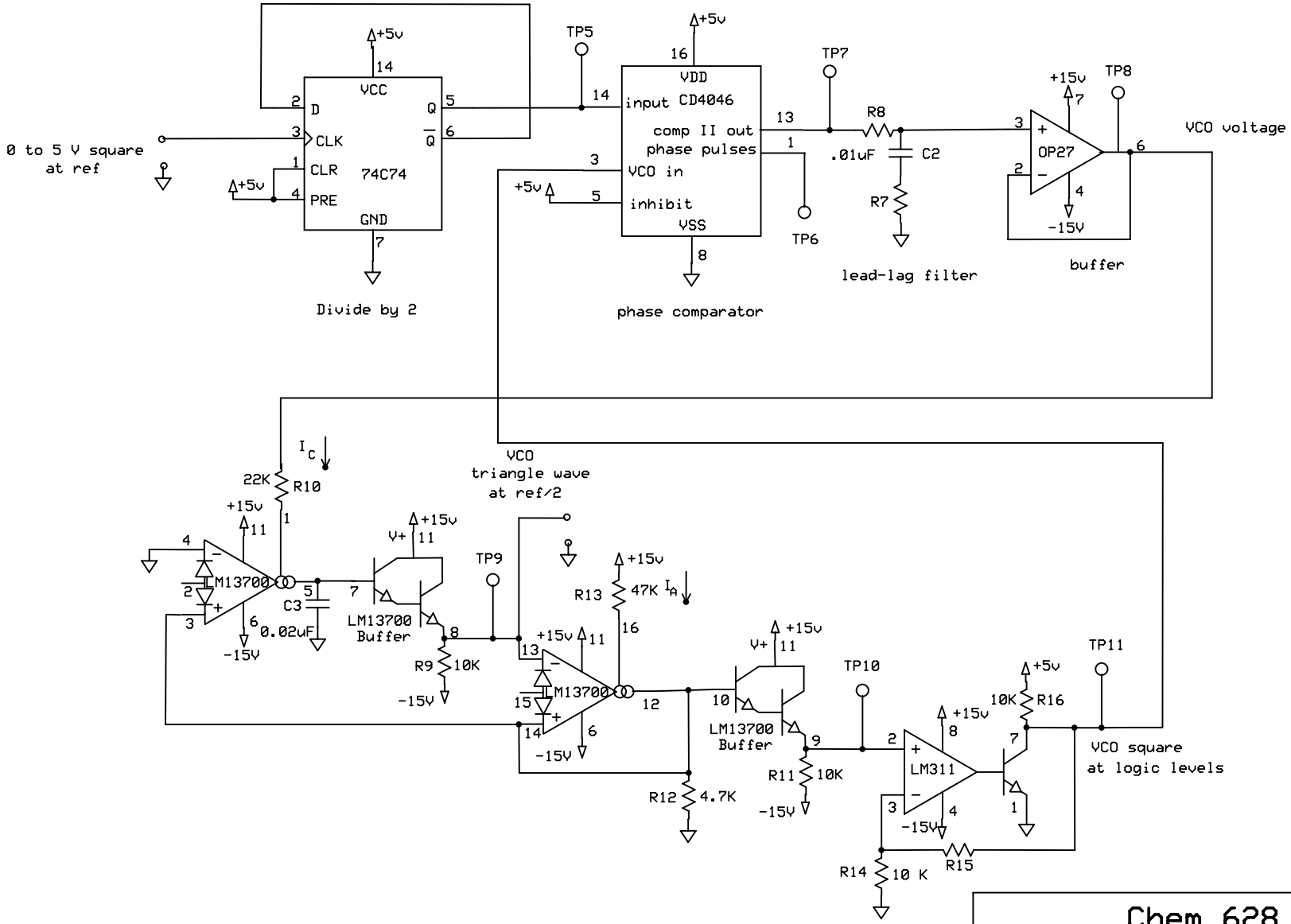


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| Divide by 2 PLL | | |
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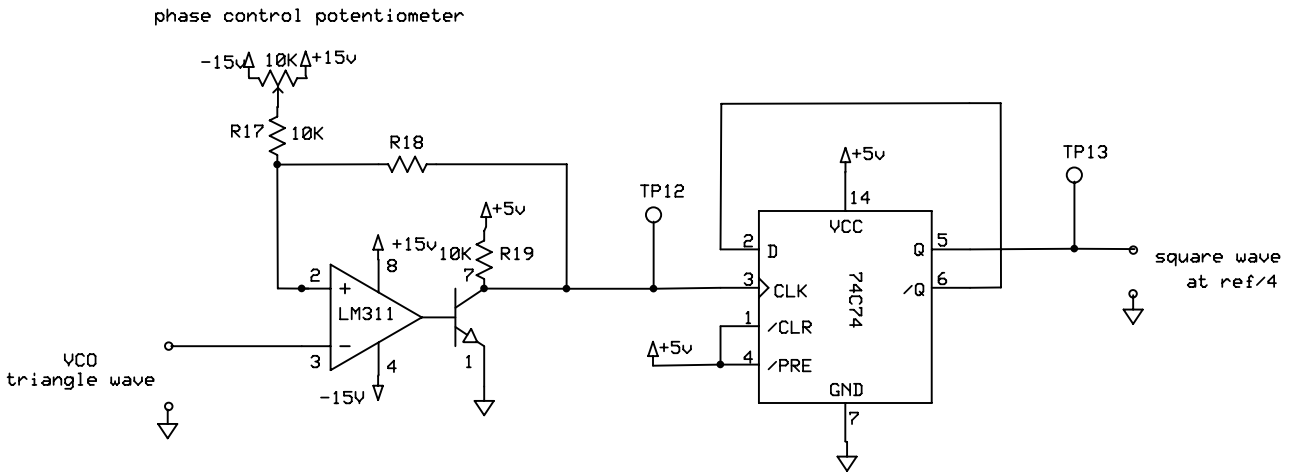


| Chem 628 Lock-in | | |
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| phase shifter | | |
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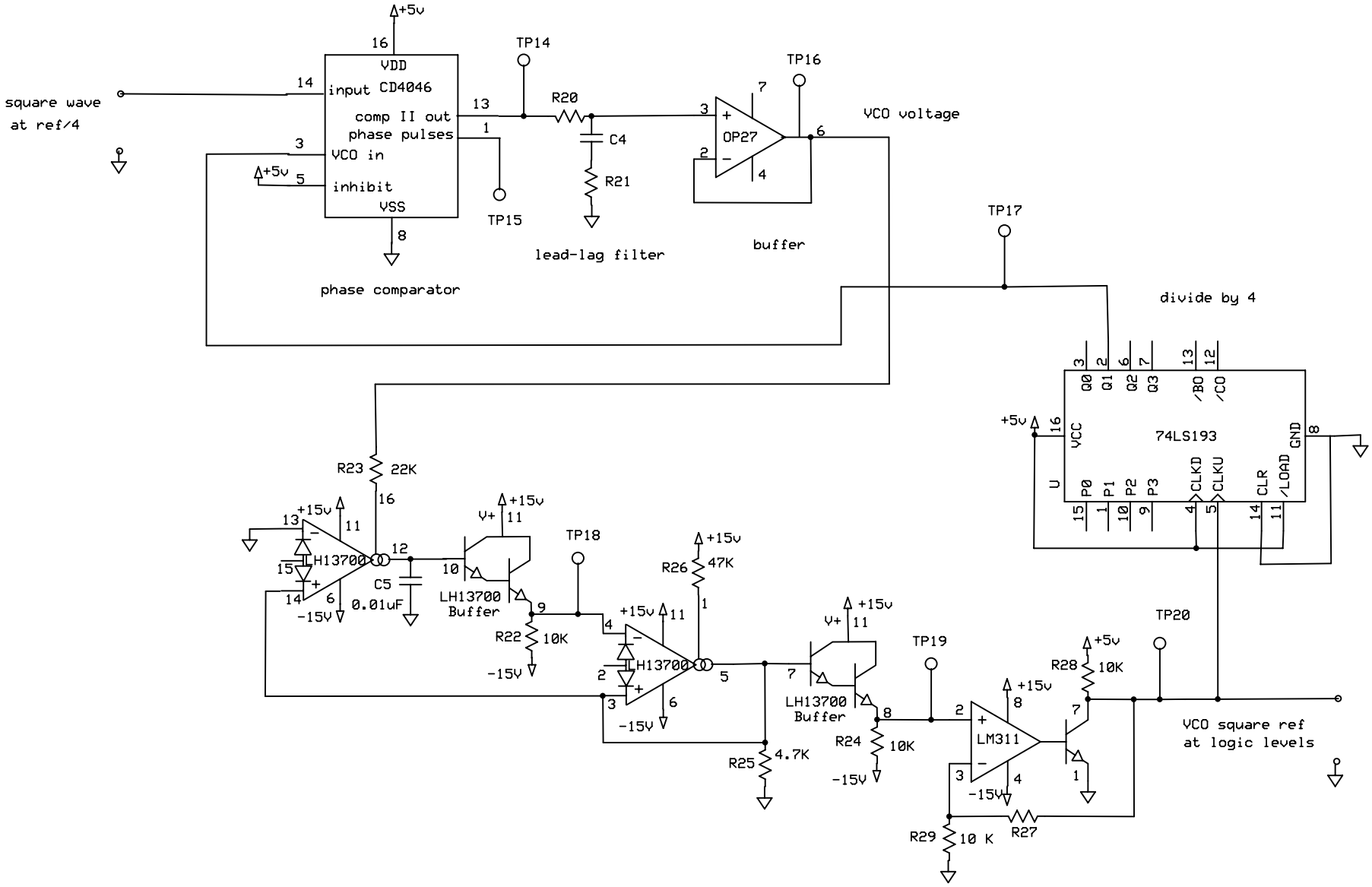


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| Multiply by 4 PLL | | |
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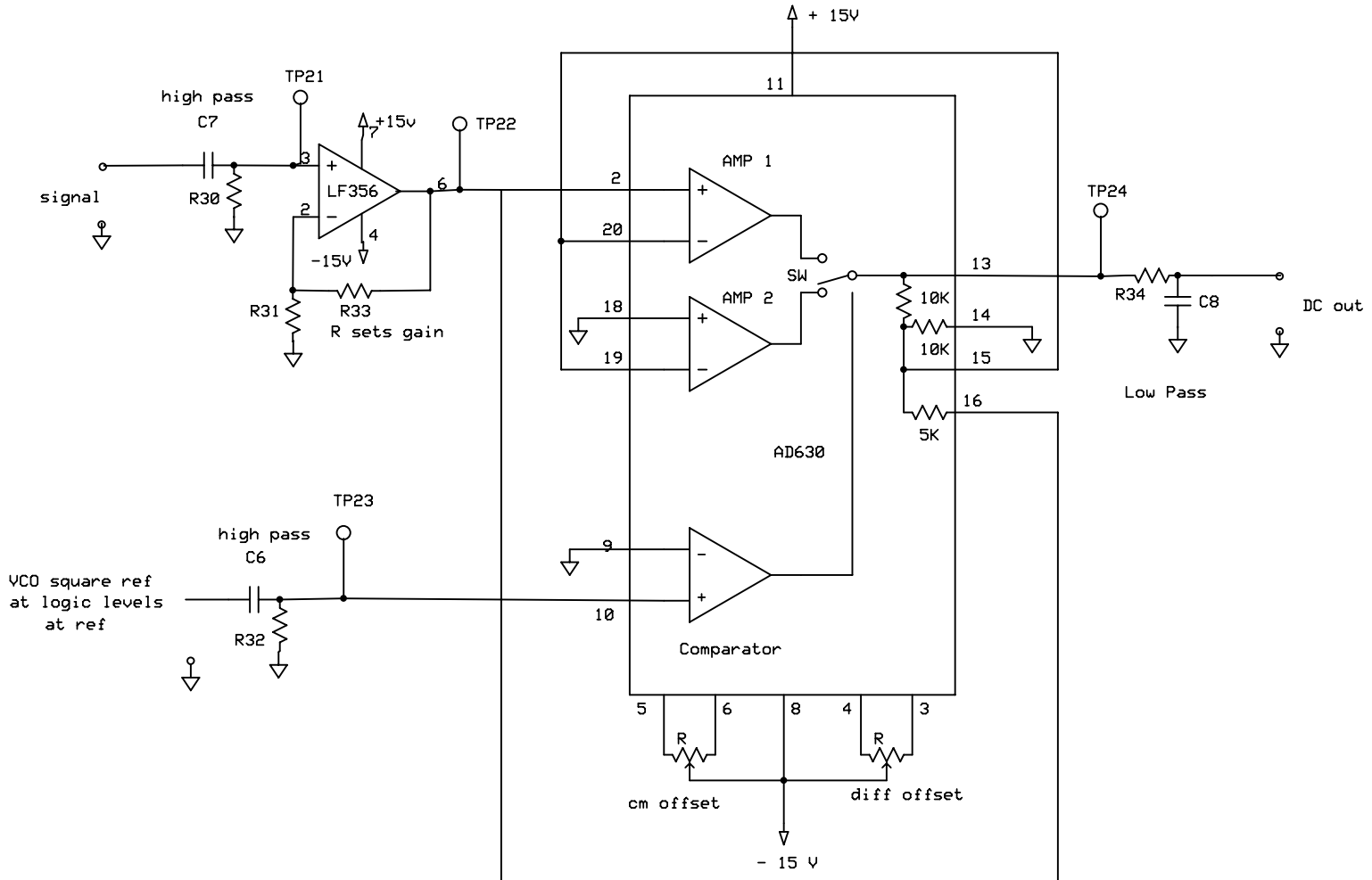


| Chem 628 Lock-in Multiplier and Filter | | |
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